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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,208	01/17/2002	Ronald Steven Niles	34826 - 1009	9084

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,208	NILES ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11,17,18 and 22-27* is/are allowed.

6)☒ Claim(s) *12-16,19,21 and 28-33* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/03,10/02,6/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13-16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "properties" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Milos et al. US PGPUB 2002/0161983.

Milos discloses a method for establishing one or more logical partitions of a memory having a memory capacity, where the one or more logical partitions define an area of the memory that is accumulatively greater than the memory capacity in paragraph 57, the method comprising:

representing the memory as a plurality of segments in figure 5 elements 508A-C and 506, each segment associated with a plurality of logical sectors in figure 6 element 608B of which the sum of the logical sectors are accumulatively greater than the memory capacity in paragraph 57;

maintaining a list of the plurality of segments available for association to the one or more logical sector addresses in figure 6 element 608B; and

establishing a data structure associated with each of the plurality of segments, the data structure defining properties of the segment in figure 6 element 606.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19, 21 and 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. US PGPUB 2004/0017707 in view of "Intel 80386 Programmer's Reference".

In regards to claim 19, Wallace discloses the request or command having a starting logical sector address and a sector count value in figure 16 elements 243 and 245, and to read data located within a range from the starting physical sector address and the ending physical sector address from the memory in figure 17B elements 273-278.

Wallace does not disclose the other specified claim limitations as set forth in claim 19.

Intel discloses a method for processing a request or command, to read data from a memory, the method comprises:

read a segment descriptor that is associated with the starting logical sector address in figure 5-2;

determine from the segment descriptor a starting physical sector address and an ending physical sector address in figure 5-3 segment base and segment limit;

Intel does not disclose the request or command having a starting logical sector address and a sector count value, and to read data located within a range from the starting physical sector address and the ending physical sector address from the memory.

Wallace's invention is the emulation of a physical disk using flash memory attached to the host via the PCMCIA standard (a PC Card in paragraph 36 and 6). PCMCIA is the principle means for expansion within a notebook computer, Nearly all notebook computers are designed around an Intel Processor or AMD (which in terms of memory management is identical to Intel's processors for code compatibility). All

references to storage (memory or disk) must undergo the virtual to physical memory translation as documented in Intel 80386 Programmer's Reference, Therefore it would have been obvious to one of ordinary skill in the art at the time of invention that Intel's memory management technique would be employed within Wallace's invention in order to provide the disk sector addresses employed within Wallace's invention.

In regards to claim 21, Intel discloses the segment descriptor comprises a physical starting sector and a second sector count value in figure 5-3.

In regards to claim 28, Wallace discloses a method for processing a request or command, having a starting logical sector address and a sector count value in figure 16 elements 231 and 233, to read data from a memory and reading the data from a location in memory that is associated with the starting logical sector address and the sector count value in figure 17B elements 273-278.

Wallace does not disclose the other specified claim limitations as set forth in claim 28.

Intel discloses reading the starting logical sector address (inherent to the processing of a virtual to physical memory translation);

determining from a group of segment descriptors a segment descriptor associated with the starting logical sector address in figure 5-2;

Wallace's invention is the emulation of a physical disk using flash memory attached to the host via the PCMCIA standard (a PC Card in paragraph 36 and 6).

PCMCIA is the principle means for expansion within a notebook computer, Nearly all notebook computers are designed around an Intel Processor or AMD (which in terms of memory management is identical to Intel's processors for code compatibility). All references to storage (memory or disk) must undergo the virtual to physical memory translation as documented in Intel 80386 Programmer's Reference, Therefore it would have been obvious to one of ordinary skill in the art at the time of invention that Intel's memory management technique would be employed within Wallace's invention in order to provide the disk sector addresses employed within Wallace's invention.

In regards to claim 29, Intel discloses wherein the determining step comprises searching a table for a segment descriptor having a logical sector address range that is associated with the starting logical sector address in figure 5-2.

In regards to claim 30, Intel discloses reading a physical starting sector address and a sector quantity from the segment descriptor in figure 5-3 segment base and segment limit;

determining physical sector addresses defined by the association of the starting logical sector address and the sector count value with the physical starting sector address and the sector quantity from the segment descriptor (inherent to the translation of the virtual addresses);

Wallace discloses reading the data located in memory at the physical sector addresses in figure 17.

In regards to claim 31, Wallace discloses a method for processing a request or command, having a starting logical sector address and a sector count value, to write data to a memory in figure 16 elements 243 and 245 and writing the data to a location in memory that is associated with the starting logical sector address and the sector count value in figure 17b elements 281-285.

Wallace does not disclose the other specified claim limitations as set forth in claim 31.

Intel discloses reading the starting logical sector address (inherent to virtual to physical memory translation);

determining from a group of segment descriptors a segment descriptor associated with the starting logical sector address in figure 5-2;

Wallace's invention is the emulation of a physical disk using flash memory attached to the host via the PCMCIA standard (a PC Card in paragraph 36 and 6). PCMCIA is the principle means for expansion within a notebook computer, Nearly all notebook computers are designed around an Intel Processor or AMD (which in terms of memory management is identical to Intel's processors for code compatibility). All references to storage (memory or disk) must undergo the virtual to physical memory translation as documented in Intel 80386 Programmer's Reference, Therefore it would have been obvious to one of ordinary skill in the art at the time of invention that Intel's memory management technique would be employed within Wallace's invention in order to provide the disk sector addresses employed within Wallace's invention.

In regards to claim 32, Intel discloses the determining step comprises searching a table for a segment descriptor having a logical sector address range that is associated with the starting logical sector address in figure 5-2.

In regards to claim 33, Intel discloses reading a physical starting sector address and a sector quantity from the segment descriptor in figure 5-3 segment base and segment limit;

determining physical sector addresses defined by the association of the starting logical sector address and the sector count value with the physical starting sector address and the sector quantity from the segment descriptor (inherent to the translation of the virtual addresses);

Wallace discloses writing the data to a location in memory associated with the physical sector addresses in figure 17B elements 273-278.

Allowable Subject Matter

Claim 1-11,17-18, 22-27 are allowed.

In regards to claims 1, 8 and 17, Milos et al. US PGPUB 2002/0161983 represents the closest available are of record. Milos discloses a system wherein physical memory is not allocated to a virtual device until a write request occurs in paragraph 56 and figure 9A, however Milos' disclosure describes the system in abstract term without disclosing how element 910 of figure 9A is performed. Milos references

application 09/665,583 (now patent 6,804,819) for the implementation of Data Propagation Platform (DPF) which is heavily relied upon in his disclosure. However this reference is the disclosure of the organization of a Storage Area Network (SAN) and provides no further information on how element 910 of figure 9A is performed. As such Milos does not disclose all claim limitations in claims 1, 8 and 17. Reuter et al. US PGPUB 2002/0019908 and Karpoff et al. US PGPUB 2002/0112113 also disclose systems where physical memory is not allocated to a virtual device until a write request occurs, but they too are deficient in the same manner as Milos in not providing a detailed disclosure of how such allocation at the time of a write request is performed. For these reasons claims 1, 8 and 17 are found allowable over the prior art of record.

Claims 2-7 and 9-11 are found allowable as being dependent upon allowed claims 1 and 8.

In regards to claim 18, Neither Intel nor Wallace discloses if the sector count does exceed the predetermined number of logical sector addresses in the segment that are available, writing data to the predetermined number of logical sector addresses in the segment that are available, determining a second starting logical sector address and a second sector count, and determining whether the second starting logical sector address is within a second segment of the one or more segments in combination with the other specified claim limitations.

In regards to claims 22 and 25, Neither Intel nor Wallace discloses if the starting logical sector address is not associated with the segment descriptor, then generate data and respond to the request or command by returning the generated data in combination with the other specified claim limitations.

Claims 23,24,26 and 27 are found allowable as being dependent upon allowed claims 22 and 25.

Claims 13-16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

12/13/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER